Computer-Aided Design Package for Designers of Digital Optical Computers

Progress Report for Grant #N00014-90-J-4018 for Period 10/1/92 - 12/31/93

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Summary

This report covers progress for the period 10/1/92 - 12/31/93 on a jointly sponsored ONR/AFOSR grant to Rutgers University which supports research into the architecture and design of digital optical computers. During this reporting period Murdocca developed the notion of a reconfigurable logic/interconnection component (RELIC) as part of an investigation into the architectural implications of reconfigurable optical interconnects. Prof. Thomas Stone made progress on the study of hybrid micro-macro optics for optical interconnection, achromatic optical interconnects, and the use of birefringent materials for optical interconnection. In addition, our experimental facilities have improved and related work has progressed at the Photonics Center at Rome Laboratory where we have found a good opportunity for technology transfer. Details of this progress are described below.

Achromatic Optical Interconnects.

One lesson that has been clearly learned from the earlier studies in this project is the highly constrained nature of the plane-to-plane optical interconnect problem. The trade-offs between gate or device spacing, required spot size, number of devices, plane separation, imaging system complexity, *etc.* are strongly related to each other and reasonable compromises immediately push optical system complexity near practical limitations. It has become increasingly apparent that using wavelength as a new dimension in order to extend the interconnect system performance without a corresponding increase in complexity is a promising direction. Further, it has been demonstrated by others that the dispersion of "single wavelength" interconnect systems can be a problem (particularly with systems utilizing diffractive elements) with the typical wavelength drift or mode hopping in sources. In response to these considerations, the topic of achromatic optical interconnection systems has been investigated.

In this area, several methods for achromatizing finite and infinite conjugate interconnects have been studied. The dispersion resulting from using simple refractive and diffractive single element lenses was characterized and compared with systems using refractive and hybrid refractive-diffractive achromats. Further, new combinations of simple dispersive elements comprising an overall achromatic interconnect system were developed. The advantage in the latter approach is that the complexity of the elements required in the system is greatly reduced over the all-achromat approaches. Typically some chromatic difference of magnification is left as a residual, but this is

not a problem in most cases and can be eliminated if required. These results are being prepared as a document for publication.

Hybrid Micro-Macro Optical Interconnects

The work with hybrid micro-macro optical interconnects described in earlier reports continued through this contract period. The concept of segmented field compensation has been passed on to another project for applied evaluation and development. Also, a novel combination of the hybrid micro-macro configuration with the achromatic results described above has been identified, and work on this topic is continuing.

Sub-Array and Redundancy Generation with Birefringent Crystals

Early in this reporting period a paper was submitted to *Applied Optics* describing the use of birefringent crystal slabs for 1) optical array generation, 2) fanout, 3) increasing the density of an existing source array, and 4) mixing the outputs of neighboring sources to reduce coherence and provide fault tolerance. The latter two are particularly useful for use with microlaser arrays that may be limited in device number or spacing (*e.g.*, by cooling considerations). This paper has been reviewed and the reviewers comments are currently being addressed. It will be returned to the editor during the beginning of the next reporting period.

Technology Transfer

During this reporting period, a related effort that supports a VCSEL/S-SEED based optical processor project at Rome Laboratory/Griffiss AFB has continued. This related effort is not charged to the current contract, but is very helpful to this contract in identifying practical problems and in gaining system experience. The laboratory facility at Rutgers is continuing to be developed, and already has appreciable capabilities (although on a very limited cost-sharing budget). During the next contract period, diffractive element fabrication capabilities will be continually improved.

Investigation into Reconfigurable Interconnects

In Murdocca's earlier work at AT&T Bell Labs, an S-SEED based architecture was customized by placing fixed masks in the image planes of the interconnects. In our current work, there is no need for the customizing masks to remain fixed, and in fact, they may be implemented in any of a number of ways, such as with ferroelectric liquid crystals, matrix addressable logic arrays, or through beam steering elements. During this reporting period, Murdocca developed the notion of a reconfigurable logic/interconnection component (RELIC) which makes use of reconfigurable optical interconnects at the gate level. In a very simple form, a RELIC consists of independently addressable optical logic gates and static optical interconnects. Reconfiguration at the gate-level is obtained by selectively enabling or disabling logic gates. A RELIC may compete with existing electronic field programmable gate arrays (FPGAs) such as the Xilinx line of reconfigurable components. The internal configuration of a Xilinx chip is shown in the left side of Figure 1. A number of programmable logic arrays (PLAs), shown as rectangles, are interconnected through an embedded arrangement of crossbar switches. The PLAs contain lookup tables (LUTs) for two seven-variable Boolean functions, and provide two bits of internal feedback to the LUTs. Each PLA generates two one-bit outputs. A small number of channels (five shown in the figure) pass through each crossbar in horizontal and vertical directions. The LUTs and crosspoints of the crossbars are configured by loading static flip/flops, one per decision element (or crosspoint). The Xilinx chips are popular in the area of rapid prototyping, in which a hardware implementation of a

target processor is realized with reconfigurable components, but at a greater cost and with reduced performance than with a custom hardware design. Commonly, Xilinx chips are used in end-products as well as in transition hardware, particularly when production quantities are small (less than 1000 units).

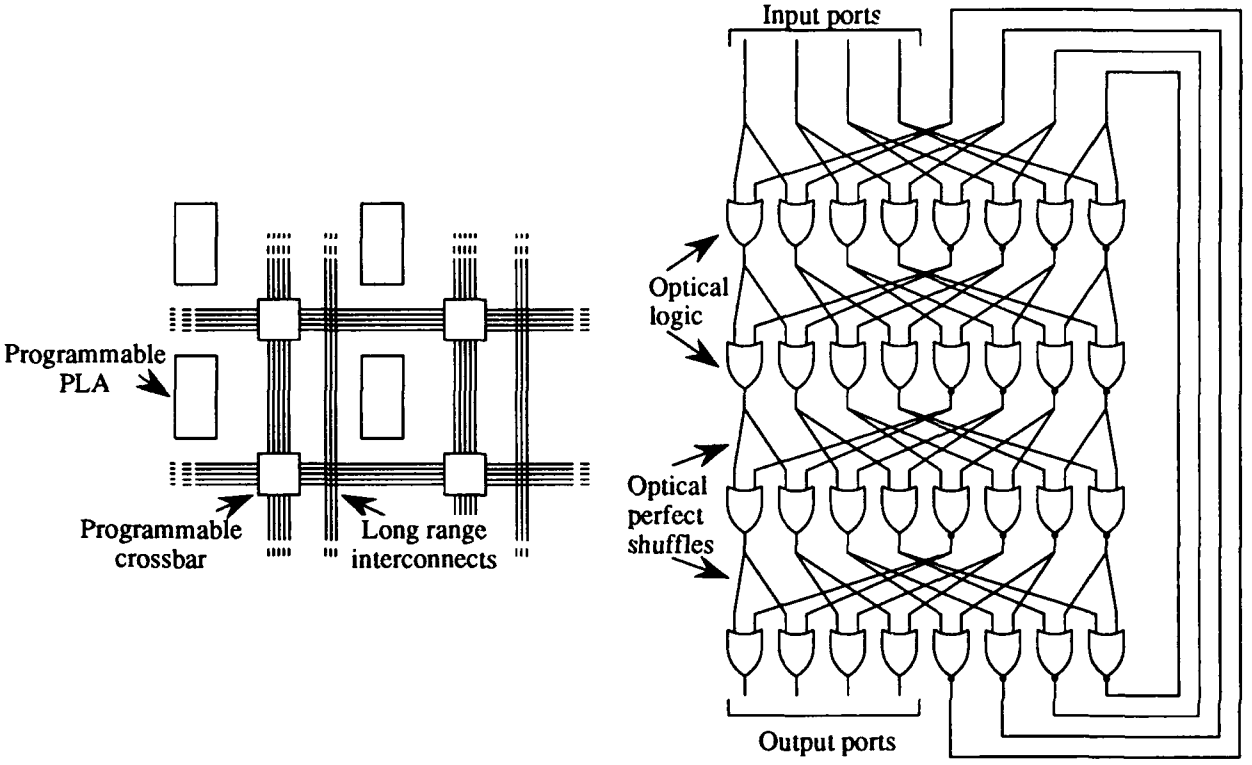


Figure 1: *Xilinx (left) and RELIC (right) models.*

With regard to reprogrammability, the Xilinx line is very flexible, but the user is forced to decompose large circuits into a number of interconnected one-bit circuits. This often unnatural decomposition sacrifices performance. For example, a ripple-carry adder maps well to the Xilinx approach, but a fast parallel adder does not. As an illustration of why this is the case, consider the general layout of a Xilinx chip, which is clustered into one-bit logic units and narrow communication channels. Although it is possible to create a gate-level switching matrix that allows a user to modify interconnects at the gate or component level, it would be nearly impossible to maintain a clock speed of 50 MHz (a typical Xilinx internal clock speed) due to the enormous wiring complexity of such a chip. The RELIC approach allows gate-level and component-level interconnects to be allocated as needed, without causing a large increase in wiring complexity. This is accomplished through a regular gate-level interconnection pattern such as a perfect shuffle, in which either the logic gates or the connections are reconfigured during operation. The gate-level layout of a RELIC is illustrated in the right side of Figure 1. We have found that gate counts using this method are higher than with for a fixed arbitrary interconnect, but that the flexibility of modifying the gate-level interconnects may override the cost in gate count.

Publications and Presentations

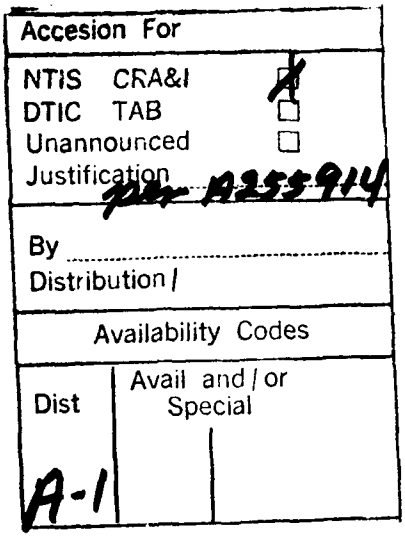
The following publication was accepted for publication during this reporting period. The ONR and AFOSR sponsoring agencies are acknowledged in the paper.

Publication

M. Murdocca, "A Case for All-Optical Digital Computing," accepted for the OSA *Topical Meeting on Optical Computing*, Palm Springs, CA, (Mar. 1993).

Plans for The Next Reporting Period

During the next (final) reporting period, Stone will continue his work on the projects described above, and he plans to submit a paper describing the achromatic optical interconnect work before the grant expires on 4/30/93. Murdocca and PhD students Vipul Gupta and Masoud Majidi will continue preparing a paper for submission to *Applied Optics* that summarizes refinements to our gate-level layout strategies. Murdocca will continue his investigation into architectural aspects of reconfigurable optical interconnects, and will prepare the final report and close-out documents for the project.



Miles Murdocca